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1 Evaluation of a virtual shared memory machine by the compilation of data parallel loops

Baiardi, F.; Guerri, D.; Mori, P.; Ricci, L.

Parallel and Distributed Processing, 2000. Proceedings. 8th Euromicro Workshop on, 1999

Page(s): 309 -316

[Abstract] [PDF Full-Text (112 KB)] CNF

2 Compiler-driven cached code compression schemes for embedded ILP processors

Larin, S.Y.; Conte, T.M.

Microarchitecture, 1999. MICRO-32. Proceedings. 32nd Annual International Symposium on , 1999

Page(s): 82 -92

[Abstract] [PDF Full-Text (120 KB)] CNF

3 ConCISe: a compiler-driven CPLD-based instruction set accelerator

Kastrup, B.; Bink, A.; Hoogerbrugge, J.

Field-Programmable Custom Computing Machines, 1999. FCCM '99. Proceedings. Seventh Annual

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5 Hardware-accelerated concurrent fault simulation: eventflow computing versus dataflow computing

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### 6 Compiler driven data cache prefetching for high performance computers

Chi-Hung Chi; Kam-Kong Fang
TENCON '94. IEEE Region 10's Ninth Annual International Conference. Theme: Frontiers of

Computer Technology. Proceedings of 1994, 1994

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### 7 Definition of timing models for compiler-driven logic simulation

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## 8 Synergy of synthesis and test (logic design)

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## 9 High-speed compiled-code simulation of transition faults

Geilert, M.

Computer-Aided Design, 1989. ICCAD-89. Digest of Technical Papers., 1989 IEEE International Conference on , 1989

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#### 10 Automated synthesis for testability

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